

97-0834

**Modification to Appendix A
of Performance Baseline
Text on MIMO Latency**

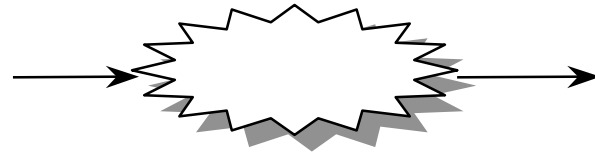
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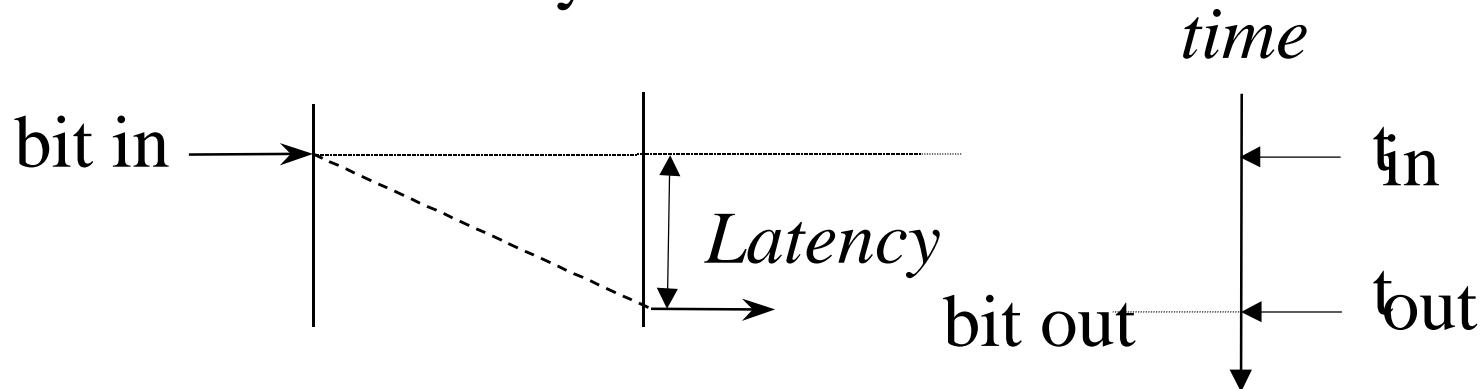


- ❑ Motivation: Why MIMO?
- ❑ Zero Delay Switch
- ❑ MIMO Latency Definition
- ❑ Examples
- ❑ MIMO Measurements
- ❑ User Perceived Delay

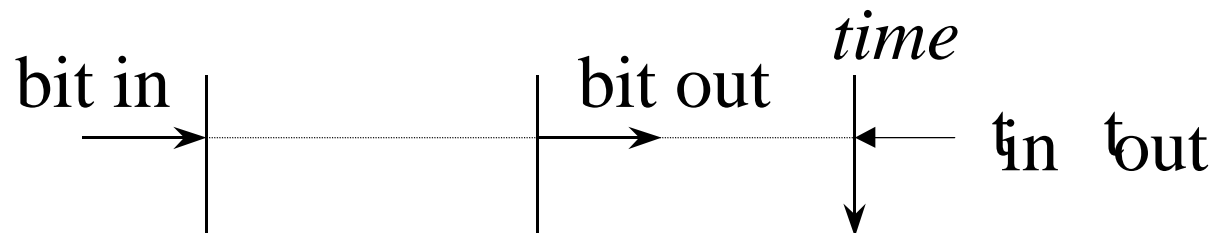
Single Bit Latency



□ Non-Zero Delay Switch:



□ Zero Delay Switch:



Usual Frame Latencies Metrics

First bit of the frame enters

Frame input time

Last bit of the frame enters

LILO

LIFO

FIFO

FILO

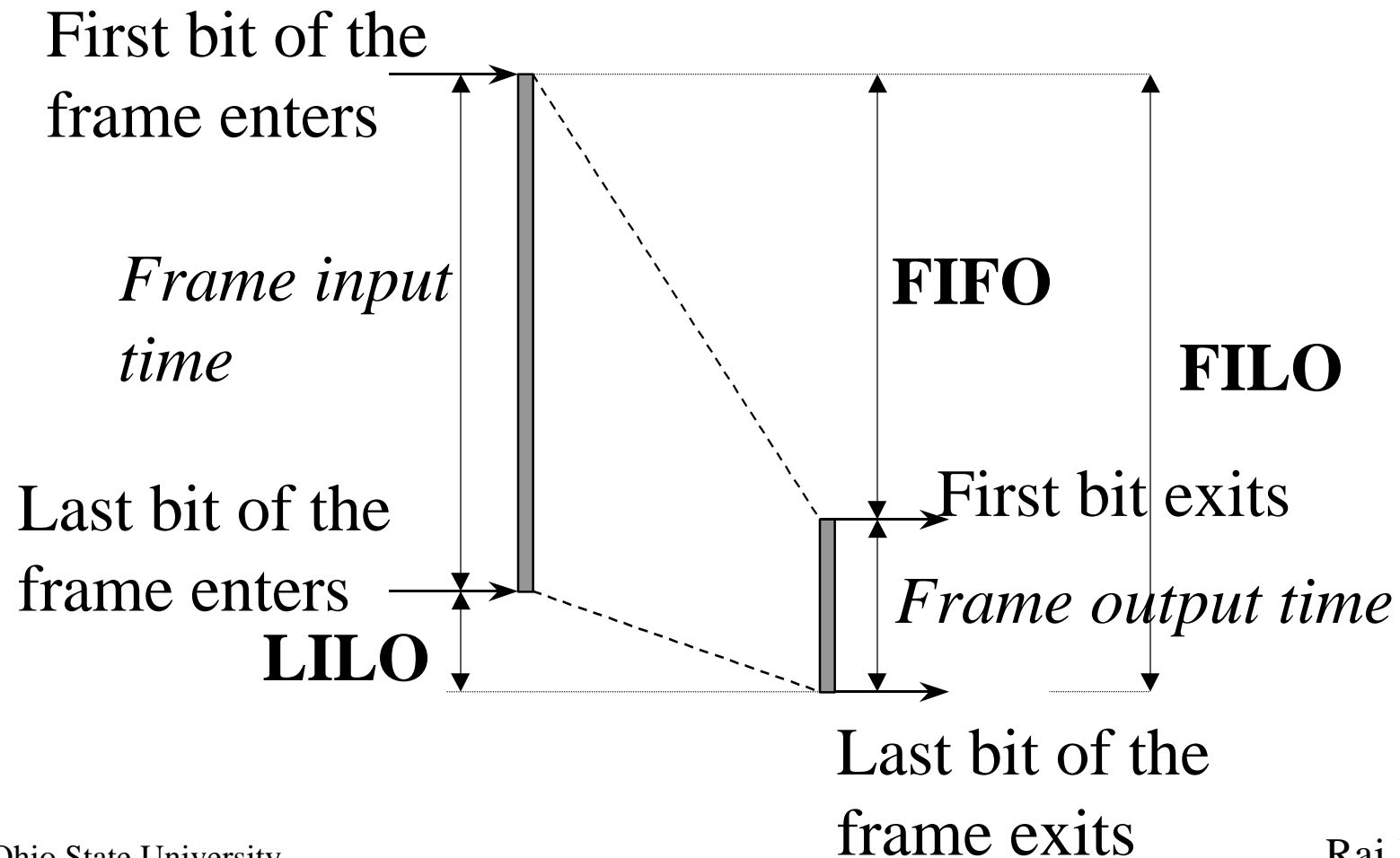
First bit exits

Frame output time

Last bit of the frame exits

LIFO

- In cut-through switches LIFO latency can be negative



FIFO

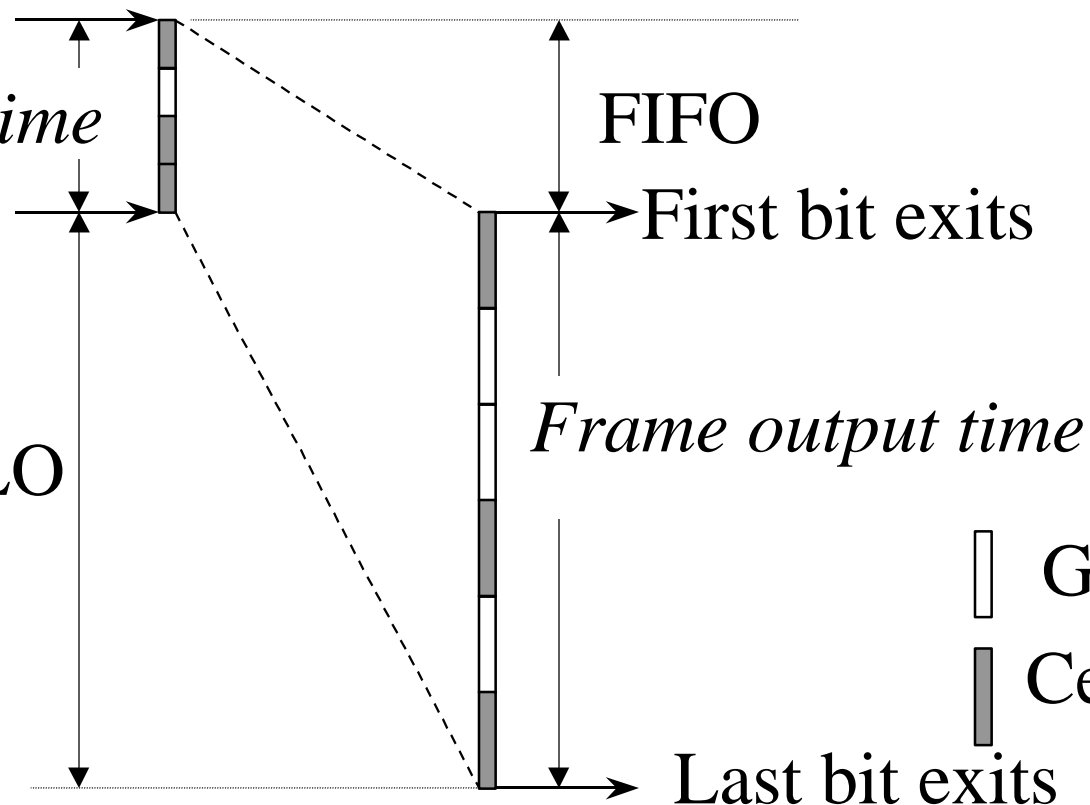
- FIFO latency may be small but the later cells may be delayed considerably

First bit enters

Frame input time

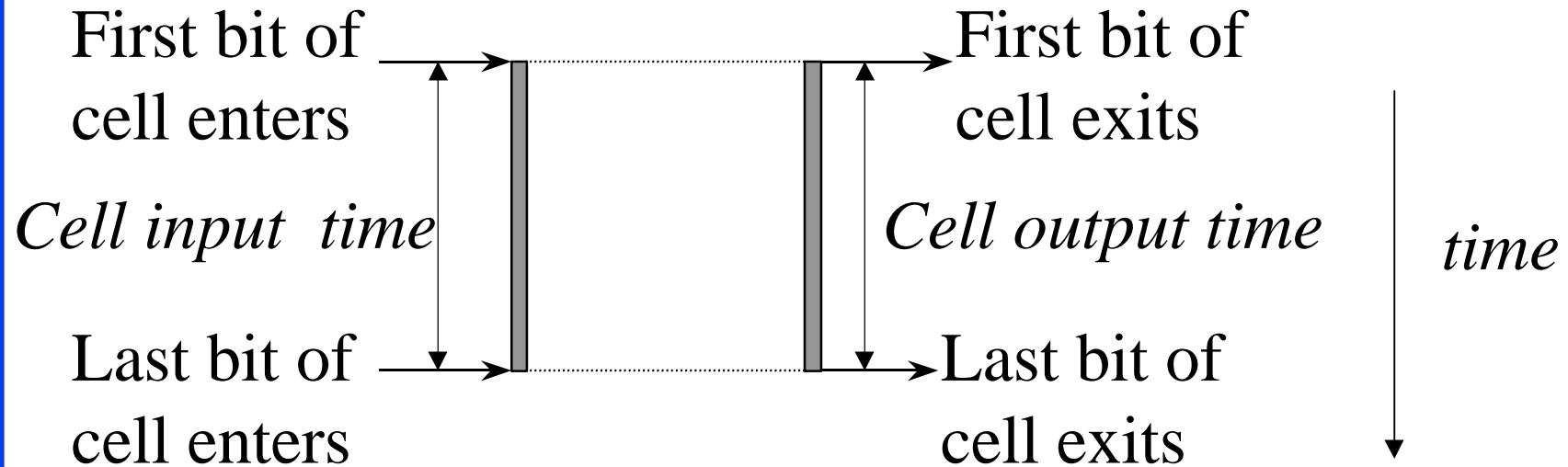
Last bit enters

LILO



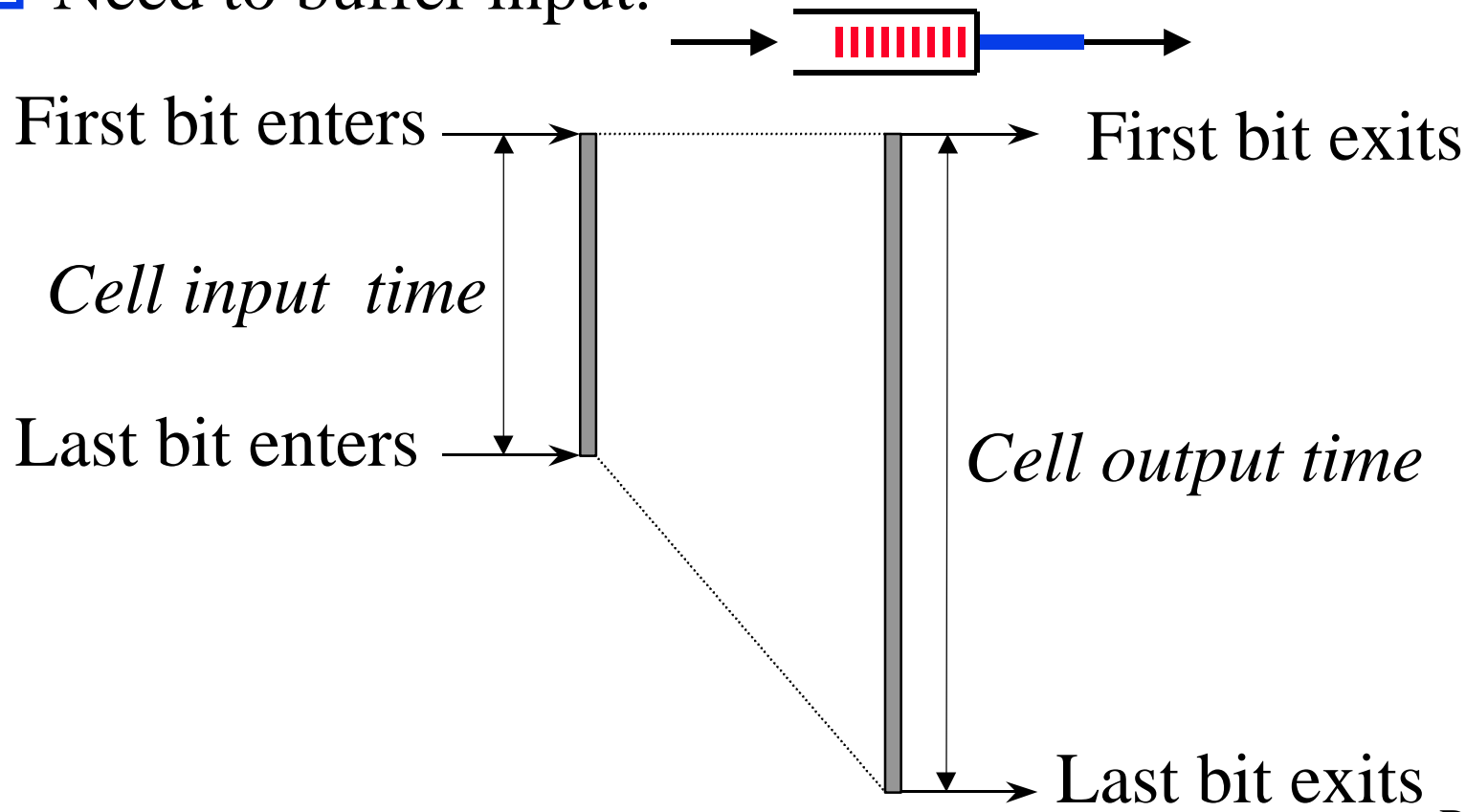
Zero-Delay Switch I

- Input Rate = Output Rate
- A fiber of length k km has a latency of $5 * k \mu\text{s}$.
- Fiber of zero length has zero latency.



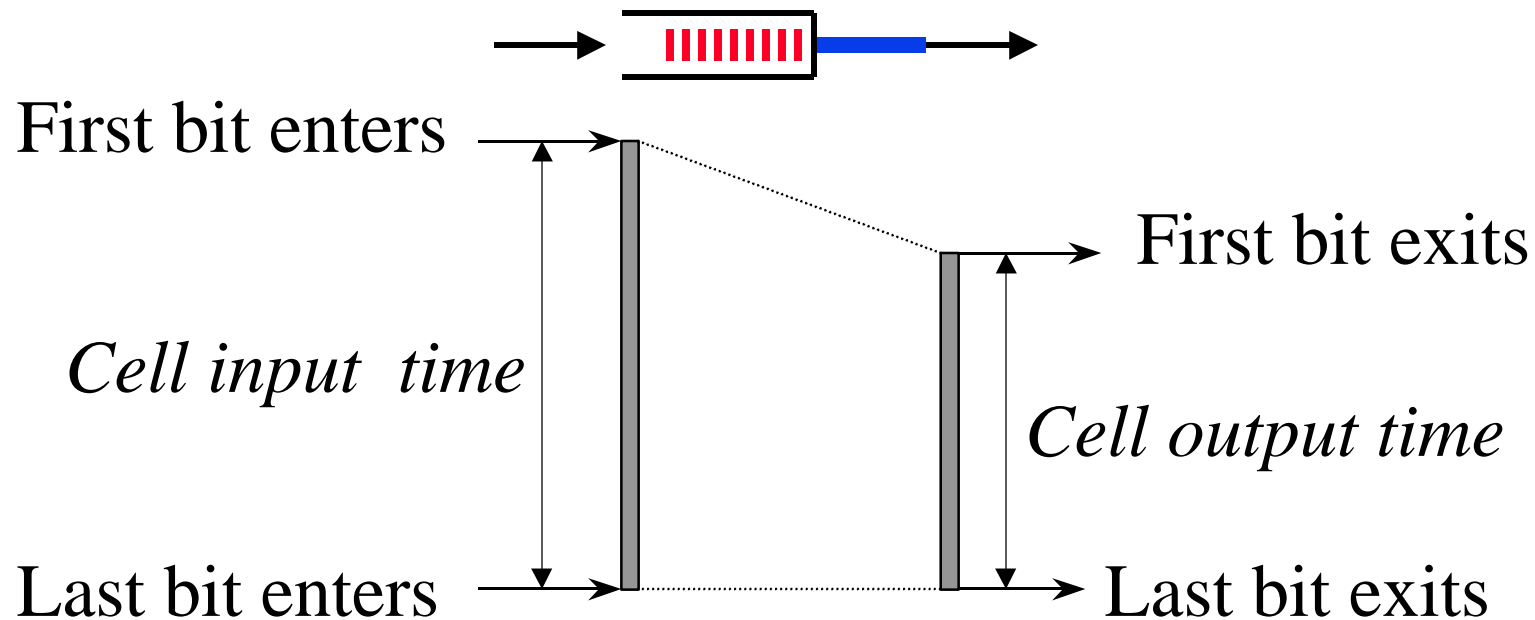
Zero-Delay Switch II

- Input Link Rate $>$ Output Link Rate
- Need to buffer input.



Zero-Delay Switch III

- Input Link Rate < Output Link Rate



- The zero-delay switch is intelligent to avoid underruns

MIMO Latency Definition

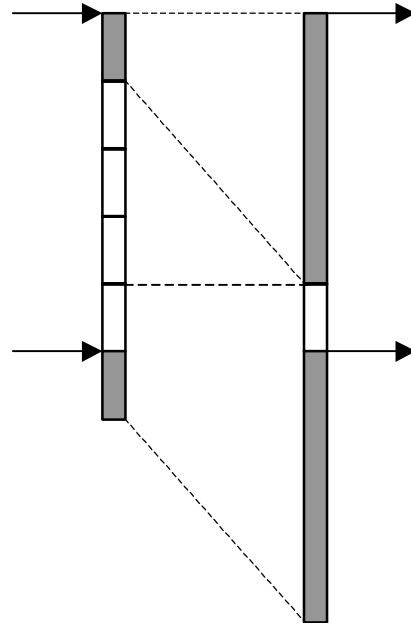
- MIMO Latency = $FILO\ Latency - NFOT$
- $FILO\ latency$ = Time between the first bit entry and the last bit exit
- $NFOT$ = Nominal Frame Output Time: the time a frame needs to pass through the zero-delay switch, calculated as:
Initially $NFOT = 0$ and time t is measured from the arrival of the first bit of the first cell. For each cell with its first bit arriving at time t
 $\Rightarrow NFOT = \max\{t, NFOT\} + CT.$
- $CT = \text{Max}\{\text{cell input, cell output time}\}$

Example 1

- Input rate $>$ Output rate
- CT = Cell Output Time = 4
- 2nd cell at 5: NFOT = $\max\{5, 4\} + 4 = 9$

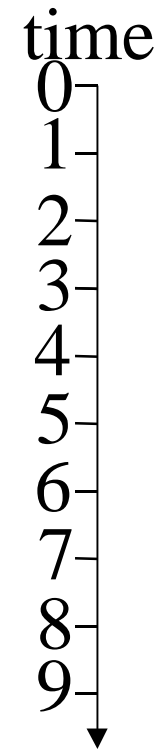
First bit of cell arrives

First bit of cell arrives



First bit of cell transmitted

First bit of cell transmitted

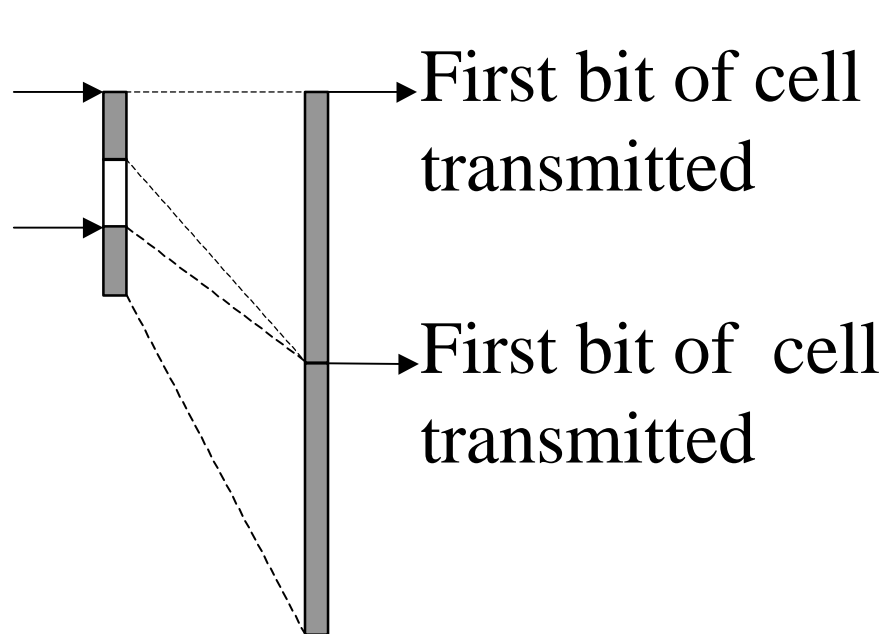


Example 2

- Input rate $>$ Output rate
- $CT = \text{Max}\{1, 4\} = 4$
- 2nd Cell arrival at 2: $\text{NFOT} = \text{max}\{2, 4\} + 4 = 8$

First bit of
cell arrives

First bit of
cell arrives

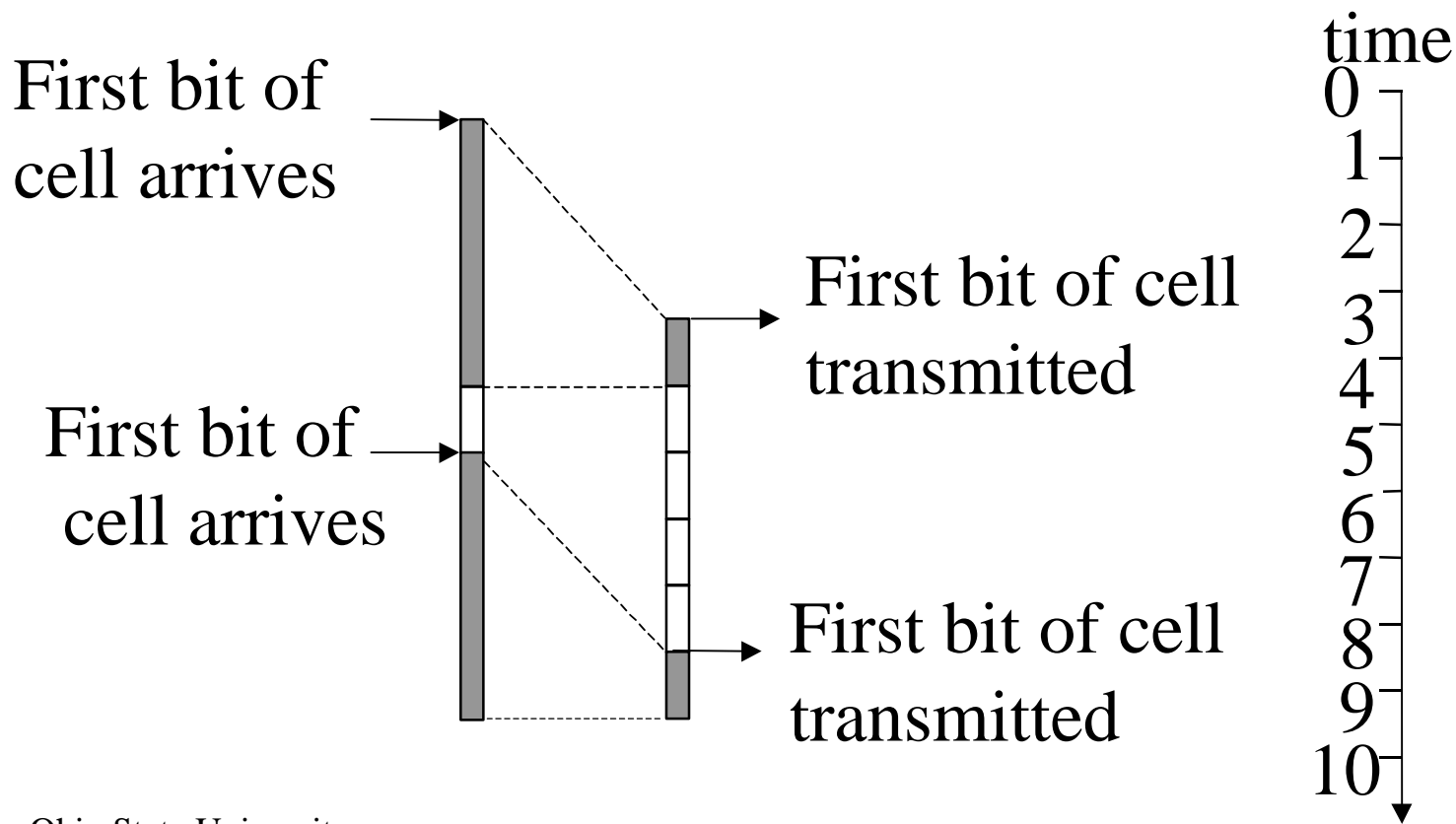


time

0
1
2
3
4
5
6
7
8
9

Example 3

- Input rate < Output rate



Equivalent MIMO Latency Definition

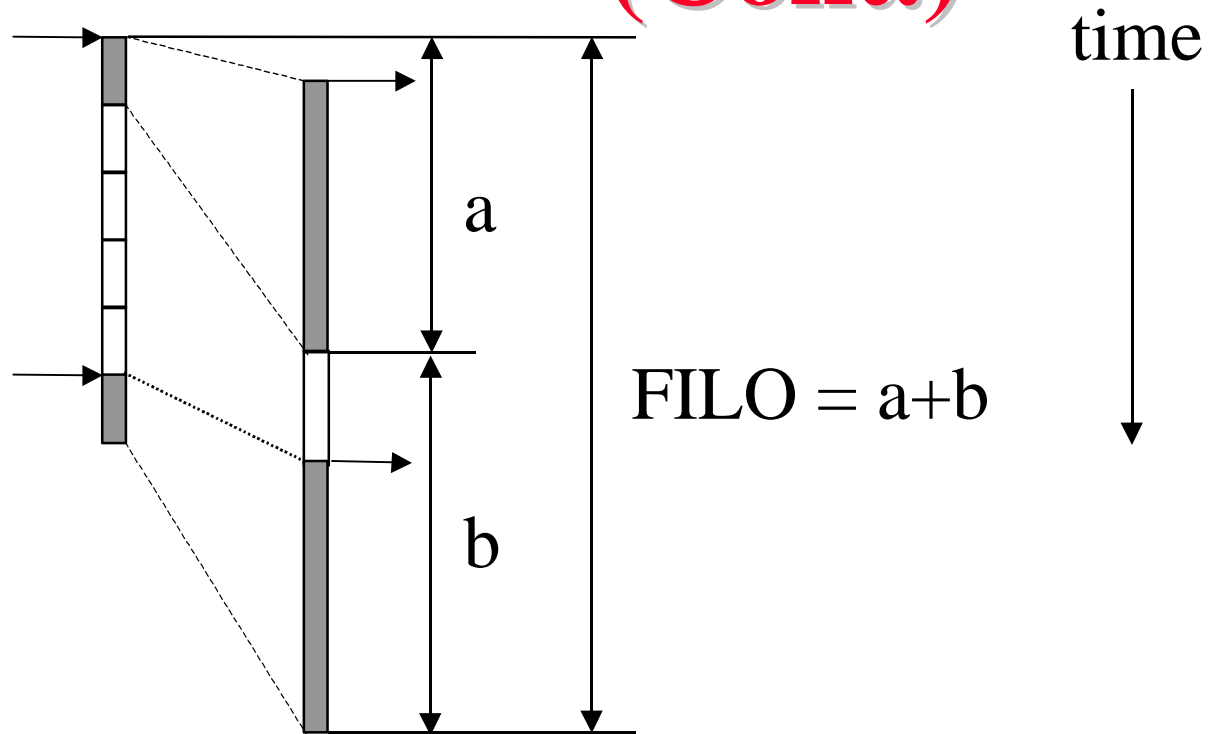
- When Input Link Rate \leq Output Link Rate:
 - $CIT \geq COT$
 - NFOT = Frame Input Time
 - $MIMO = FILO \text{ Latency} - NFOT$
 $= FILO \text{ Latency} - \text{Frame Input Time}$
 $= \mathbf{LILO}$

$$MIMO = \begin{cases} FILO - NFOT, & \text{if Input rate} > \text{Output rate} \\ LILO, & \text{otherwise} \end{cases}$$

Practical MIMO Measurements

- Contemporary ATM Monitors provide measurements data at the cell level:
 - Cell Transfer Delay (CTD)
 - Cell Inter-Arrival Time
- From the next slide:
FILO = First Cell Transfer Delay +
+ First Cell to Last Cell inter-arrival time
- Then, calculate NFOT and obtain MIMO as:
$$\text{MIMO} = \text{FILO} - \text{NFOT}$$

Practical MIMO Measurements (Cont.)

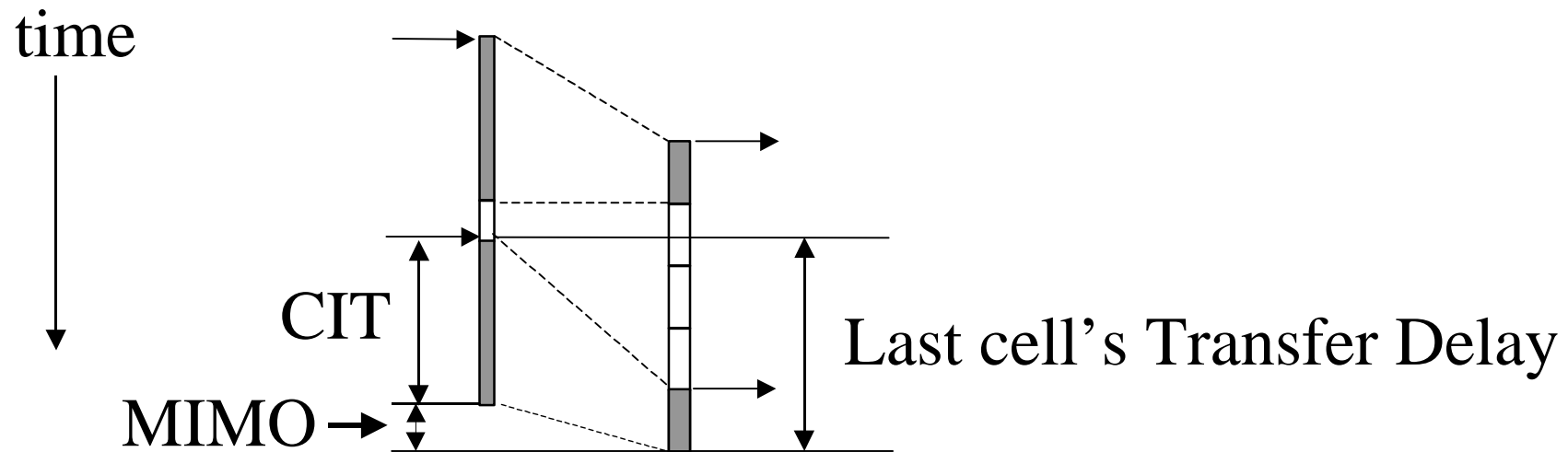


a = First Cell Transfer Delay

b = First Cell to Last Cell inter-arrival time

Practical MIMO Measurements (Cont.)

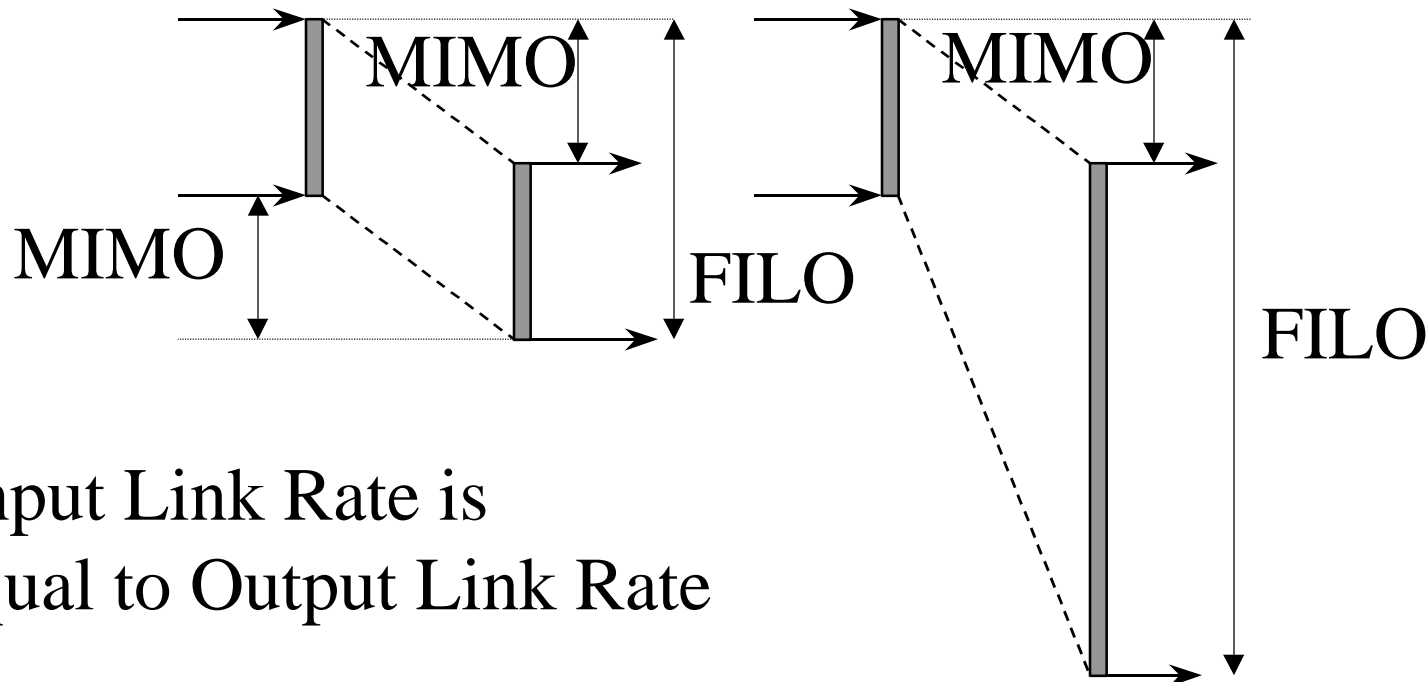
- If Input Link Rate \leq Output Link Rate:
 - MIMO = LILO = Last cell's Transfer Delay - CIT



User Perceived Delay

- ❑ The user starts waiting as soon as the first bit starts entering the system until the last bit exits the network.
- ❑ So, user perceived performance is reflected by FILO Latency
- ❑ MIMO latency measures only the switch's contribution to the delay

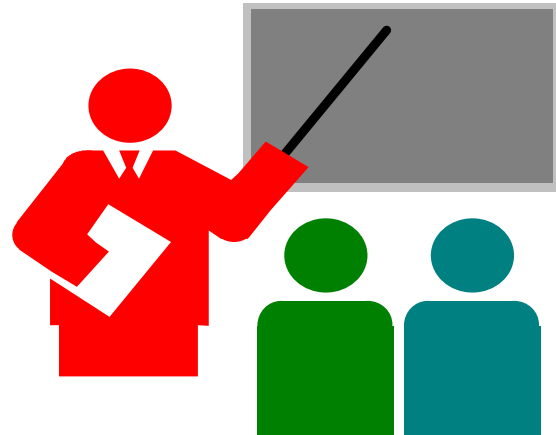
User Perceived Delay (Cont)



a. Input Link Rate is equal to Output Link Rate

b. Input Link Rate is greater than Output Link Rate

Summary



- ❑ Usual frame latencies are not appropriate for ATM systems.
- ❑ User perceive FILO latency as network delay
- ❑ MIMO measures the switch component of FILO
- ❑ MIMO Latency can easily measured using contemporary ATM monitors.

Motion

- Adopt the text under heading “Modifications to Appendix A of Performance Testing Baseline Text on MIMO latency” of 97-0834 to replace Appendix A of Performance Testing Baseline Text.