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Title: Effect of VS/VD on Switch Buffer Requirements

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Abstract:

In this contribution, we present simulation results on the effect of Virtual Source/Virtual Destination(VS/
WAN/satellite configurations show that the ABR buffer requirements in the switch are bounded by the prev
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1. Introduction

In ABR traffic management the control loop is an end-to-end loop. All the resource management (RM) cells are sent from the source to the destination and then returned back to the source. Therefore, it may take as long as one round trip time (RTT) for these RM cells to affect the available cell rate (ACR) of the source. In the ATM Forum Traffic Management Specification Version 4.0 [1], Virtual Source/Virtual Destination (VS/VD) is proposed to allow the control loop to be segmented into several shorter control loops. A VS works like a real source in the sense that it controls the transmission rate of the virtual circuit (VC) just as a real source does. Similarly, a VD works like a real destination. A single switch can be both a VD for the previous control loop and a VS for the next control loop. As a result, the end-to-end control is replaced by segment-by-segment control.

In our previous study [4], it was shown that VS/VD can reduce the response time during the first round trip and improve convergence time. In this study, we extend our work on VS/VD by studying its effect on switch buffer requirements.

This contribution is organized as follows. Section 2 briefly describes the switch and VS/VD algorithms implemented. Then, we describe the simulation set-up, which includes the switch algorithm parameters, VS/VD options, and different configurations for our simulation. Finally, we present simulation results and their analysis in section 4.

2. Design and Implementation of VS/VD

The simulations are based on our switch algorithm, Explicit Rate Indication for Congestion Avoidance (ERICA+), and our implementation of VS/VD. For detailed information about the algorithm, see [2], [3] and [4].

The ERICA+ algorithm allocates only a fraction of the total available capacity and the remaining capacity is used to drain queues. The fraction allocated is a function of the target queuing delay at the switch. Whenever the real queuing delay exceeds the target queuing delay, ERICA+ reduces the allocated ABR capacity. This reserves more bandwidth to drain the queue. If the actual queuing delay is smaller than this parameter, ERICA+ increases the allocated ABR capacity, which, in turn, increases the link utilization.

A number of design alternatives for VS/VD were studied in [4]. After an extensive simulation study, it was concluded that the best design is one in which the VC's rate is measured at the output of the per-class queue, in the next loop, the total link input rate is measured at the input of the per-class queue in the next loop. Also, when a link becomes congested, the switch reduces the ER in both the next and the previous control loops. The rate allocation is recomputed both when an FRM is received on the previous loop and when a BRM is received on the next loop. This is the design that we used in the simulations reported here.

3. Simulation Set-up

VS/VD has little effect on the performance of LAN configurations. Therefore, in this study we consider only WAN

configurations. The use of satellite links highlights the effect of feedback delays. Because of the large delay-bandwidth paths, the queues in the switches can be large. Normally, the satellite (ground) switches are designed with large buffers to allow for the large link delay. Other switches may not have that large buffers. We, therefore, purposely chose configurations in which the switch connected to the satellite links was not the bottleneck. We used three different such configurations.

Configuration 1:

In this configuration, there are 5 sources sending to 5 destinations. The connection from each source to its corresponding destination crosses 3 switches as shown in Figure 1.
LINK2 is the bottleneck because its bandwidth is 45 Mbps while all other links are 155 Mbps.

The one-way link latencies are as follows:
L1 (Src to SW1) = 275ms, LINK1 = 5ms, LINK2 = 5ms,
L2 (SW3 to Dest) = 5us

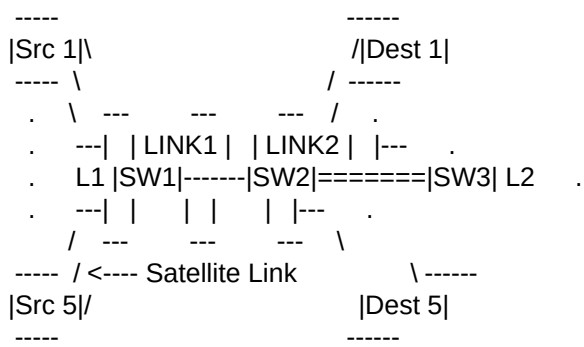

Figure 1: Five sources/three switches configuration

The purpose of this configuration is to see whether the bottleneck queues are proportional to the total roun difference.

Configuration 2:

Here, we also have 5 connections, but each connection goes through 4 switches. The connections are bottlenecked at LINK3. See Figure 2.

The one-way link latencies are as follows:
L1 (Src to SW1) =5us, LINK1=275ms, LINK2=5ms, LINK3=5ms,
L2 (SW4 to Dest)=5us

LINK3 is a 45.0 Mbps link, while all other links are 155.52 Mbps.

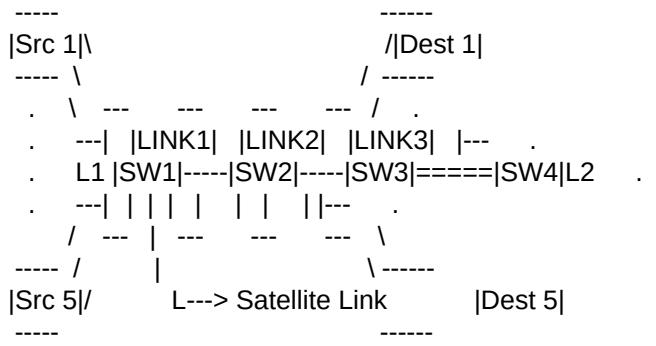

Figure 2: Five sources/four switches configuration

Configuration 3:

This is the same as configuration 2. The only difference is that the latency of the link between SW2 and D
senstivity to the previous loop's delay.

Parameter Settings:

The following parameter values are used:

-- All link bandwidths are 155.52 Mbps unless specified;

-- All sources are infinite TCP sources;

-- All buffers are infinite. There is no cell loss during the simulation. This enables us to measure the maxim

-- Peak Cell Rate is 155.52 Mbps;

-- Initial Cell Rate(ICR) for TCP source configurations is 10 Mbps;

-- All simulations run for 15 seconds;

-- TCP timer granularity is 100 ms;

-- TCP window size is 34,000 with a scale factor of 8, i.e., the real window size is 34,000 * 256. This ensu

-- The traffic is unidirectional. The sources send data. The destinations send only acknowledgments.

4. Simulation Results

The simulation results are shown in the following tables. In each table, the first column shows the options u
configuration: ERICA+ without VS/VD, and ERICA+ with VS/VD. The remaining columns show the ma
VS/VD requires per-VC queues and so there are several queues in the switch. The queue size reported h

Table 1, Table 2, and Table 3 are the simulation results for configuration 1, configuration 2, and configuration 3, re

Table 1: Maximum Queue Sizes of Configuration 1

Options	Max Switch1 Queue Size (cells)	Max Switch2 Queue Size (cells)	Max Source Queue Size (cells)
ERICA+ w/o VS/VD	3,267	61,615	73,000
ERICA+ w. VS/VD	7,100	4,700	70,000~160,000

Table 2: Maximum Queue Sizes of of Configuration 2

Options	Max Switch1 Queue Size (cells)	Max Switch2 Queue Size (cells)	Max Switch3 Queue Size (cells)	Max Source Queue Size (cells)

ERICA+ w/o VS/VD	433	2	61,094	74,000
ERICA+ w. VS/VD	95	10,200	9,000	73,500~154,000

Table 3: Maximum Queue Sizes of Configuration 3

Options	Max Switch1 Queue Size (cells)	Max Switch2 Queue Size (cells)	Max Switch3 Queue Size (cells)	Max Source Queue Size
ERICA+ w/o VS/VD	384	2	61,157	29,300
ERICA+ w. VS/VD	113	8,000	8,800	33,000

Note that in the non-VS/VD case, the bottlenecked switches, which are Switch2 in table 1 and Switch3 2 sources with an ICR of 10 Mbps, and a bottleneck capacity of 45 Mbps, the input/output bandwidth diff Thus, the product of the feedback delay and the input/output bandwidth difference is 5 Mbps * 560 ms, w times as big as this.

For the VS/VD case, the previous switches before the bottlenecked switches have large queue size. In s delay (550ms) times input/output bandwidth difference (5 Mbps), which is 6,500 cells. In table 2 and tab these are between 1 and 2 times of the above product.

The only difference between configuration 2 and 3 is the latency of LINK2. The former is 5ms, the latter is delay of configuration 2 is 10ms larger than configuration 3, the queue sizes at the switches following LINK2 VS/VD and VS/VD case.

Observe that VS/VD moves part of the queue to the edge of the network. In table 1, the source queue 70,000 (from 70,000 to 160,000) in the VS/VD case. In table 2, the source queue size increases from 74,0 increase from 29,300 to 33,000.

From the above simulation results, it appears that for a non-VS/VD switch, the maximum ABR queue siz delay and link bandwidth. Since the feedback delay changes with different connections, this size also va because depending on its connections, the maximum buffer requirements are different.

For a VS/VD switch, however, the queue size is bounded by the product of the previous loop delay and i can provide feedback on its congestion status to the previous switch in just the previous loop delay. V transmission rate. Therefore, the queue size in the bottleneck switch is bounded. However, the previous first bottleneck switch, this switch can also pass this congestion information to its previous switch. As a r one step, the degree of congestion is reduced. If the network cannot entirely manage the congestion, par

Since the previous hop delay and the link bandwidth of a switch are known when it is connected to a ne and fixed.

Generally, the buffer requirements of a VS/VD switch are bounded by the maximum of the product of its p loop delay and link bandwidth. The former is used to avoid cell loss, as explained above, while the latter of this situation is when ABR traffic is sharing a link with a higher priority VBR burst. When the VBR goe available bandwidth.

5. Conclusion

In this contribution, we show by simulations that without VS/VD, the bottlenecked switch queue size ca and feedback delay. Therefore, the switch queue size is a function of the network diameter. With VS/VD Normally, the maximum queue size at a switch is the product of its previous loop delay and the differe appears that with VS/VD, the maximum buffer requirements of a switch are bounded by the link bandwidt a VS/VD switch can be easily predicted.

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